CLAIMS

1. A semiconductor structure, comprising:

a raised source;

a raised drain; and

a gate located between said source and said drain, said gate defining a first gap between said gate and said source, and said gate defining a second gap between said gate and said drain.

2. The structure of claim 1 wherein said raised source includes doped polysilicon.

3. The structure of claim 1 wherein said raised drain includes doped polysilicon.

4. The structure of claim 1 wherein said gate includes doped polysilicon.

5. The structure of claim 1 further comprising a capping layer, said capping layer closing said gaps.

6. The structure of claim 1 further comprising a first junction area located beneath said first gap and a second junction area located beneath said second gap.

7. The structure of claim 1 wherein said first gap is approximately 100 to 500 Å wide.

8. The structure of claim 1 wherein said second gap is approximately 100 to 500 Å wide.

9. The structure of claim 1 wherein said source includes a plug.

10. The structure of claim 9 wherein said plug includes an adhesive layer.

11. The structure of claim 1 wherein said gate includes a gate terminal.

12. A semiconductor structure formed on a substrate assembly, comprising:

a raised source;

a raised drain;

a gate located between said source and said drain, said gate defining a first gap between said gate and said source, and said gate defining a second gap between said gate and said drain;

a first junction area located in the substrate assembly beneath said first gap; and

a second junction area located in the substrate assembly beneath said second gap.

13. The structure of claim 12 wherein said first and second junction areas include doped silicon areas.

14. The structure of claim 13 wherein said doped silicon areas include phosphorous.

15. The structure of claim 12 wherein said first and said second junctions extend beneath said gate, said source, and said drain.

16. The structure of claim 12 wherein said first and second junctions include pocket implant junctions.

17. A transistor formed on a substrate assembly, comprising:

a gate structure;

a raised drain structure;

a raised source structure;

a first junction area in the substrate assembly between said gate structure and said raised drain structure, said first junction area extending beneath said gate structure and said raised drain structure; and

a second junction area in the substrate assembly between said gate structure and said raised source structure, said second junction extending beneath said gate structure and said raised source structure.

18. The transistor of claim 17 further comprising a capping layer located on the substrate assembly, and wherein said capping layer defines a first capped gap located between said gate structure and said raised drain structure and wherein said capping layer

defines a second capped gap located between said gate structure and said raised source structure.

19. The transistor of claim 17 wherein said first and second junctions include doped areas.

20. A transistor, comprising:

a gate;

a raised drain;

a raised source;

first means for reducing the capacitance between said gate and said raised drain; and

second means for reducing the capacitance between said gate and said raised source.

21. The transistor of claim 20 wherein said first means for reducing the capacitance includes a capping layer forming an upper boundary of a gap between said gate and said drain.

22. The transistor of claim 20 wherein said second means for reducing the capacitance includes a capping layer forming an upper boundary of a gap between said gate and said source.

23. The transistor of claim 20 wherein said first means for reducing the capacitance includes a capped gap.

24. The transistor of claim 20 wherein said second means for reducing the capacitance includes a capped gap.

25. The transistor of claim 20 further comprising means for providing a conductive path between said gate structure and said raised drain structure.

26. The transistor of claim 25 wherein said means for providing a conductive path includes a junction.

27. The transistor of claim 20 further comprising means for providing a conductive path between said gate structure and said raised source structure.

28. The transistor of claim 26 wherein said means for providing a conductive path includes a junction.

29. A transistor, comprising:

a gate structure;

a raised drain structure;

a raised source structure;

first means for providing a conductive path between said gate structure and said raised drain structure; and

second means for providing a conductive path between said gate structure and said raised source structure.

30. The transistor of claim 29 wherein said first and second means for providing a conductive path include doped areas.

31. The transistor of claim 29 further comprising means for reducing the capacitance between said gate structure and said raised drain structure.

32. The transistor of claim 29 further comprising means for reducing the capacitance between said gate structure and said raised source structure.

33. A semiconductor structure located on a substrate assembly, comprising:

a gate structure;

a raised drain structure located adjacent said gate structure, said raised drain structure defining a gap located between said gate structure and said raised drain structure;

a raised source structure located adjacent said gate structure; said raised source structure defining a gap located between said gate structure and said raised source structure; and

a capping layer formed on the substrate assembly.

34. The structure of claim 33 wherein said capping layer includes an insulative layer.

35. The structure of claim 33 wherein said capping layer includes an oxide layer.

36. The structure of claim 33 further comprising an insulative layer on the capping layer.

37. A transistor, comprising:

a substrate layer;

a gate structure;

a first doped polysilicon area located adjacent said gate structure, said first doped polysilicon area defining a gap located between said gate structure and said first doped polysilicon area;

a second doped polysilicon area located adjacent said gate structure, said second doped polysilicon area defining a gap located between said gate structure and said second doped polysilicon area;

a first pocket implant area in said substrate layer, said first implant area located beneath said first doped polysilicon area;

a second pocket implant area in said substrate layer, said second implant area located beneath said second doped polysilicon area; and

a capping layer, said capping layer closing said gaps.

38. The transistor of claim 37 wherein said gate structure includes doped polysilicon.

39. The transistor of claim 37 wherein said first doped polysilicon area includes a drain structure.

40. The transistor of claim 37 wherein said second doped polysilicon area includes a source structure.

41. The structure of claim 37 wherein said first and second pocket implant areas include phosphorous.

42. The structure of claim 37 further comprising an insulative layer above said capping layer.

43. The structure of claim 37 further comprising at least one contact area connected to one of said gate, said drain, and said source.

44. The structure of claim 42 further comprising at least one metallization layer above said contacts.

45. The structure of claim 44 wherein said metallization layer includes aluminum.

46. The structure of claim 44 wherein said metallization layer includes copper.

47. A method of forming a semiconductor structure on a substrate assembly, the substrate assembly having a gate, comprising:

forming a sacrificial layer on the substrate assembly;

removing a portion of said sacrificial layer to form at least one spacer adjacent said gate;

forming raised source and drains on the substrate assembly; and

removing said spacer.

48. The method of claim 47 wherein forming a sacrificial layer includes forming a dielectric layer.

49. The method of claim 47 wherein forming a sacrificial layer includes forming a nitride layer.

50. The method of claim 47 wherein forming a sacrificial layer includes depositing a nitride layer.

51. The method of claim 47 wherein forming a sacrificial layer includes forming a photoresist layer.

52. The method of claim 47 wherein forming a sacrificial layer includes forming a polyimide layer.

53. The method of claim 47 wherein forming a sacrificial layer includes forming an SOG layer.

54. The method of claim 47 wherein removing a portion of said sacrificial layer includes etching said sacrificial layer.

55. The method of claim 47 wherein forming raised source and drains includes forming polysilicon areas.

56. The method of claim 55 wherein forming raised source and drains includes etching said polysilicon areas.

57. The method of claim 56 wherein forming raised source and drains includes doping said etched polysilicon areas.

58. The method of claim 57 wherein forming raised source and drains includes doping said etched polysilicon with phosphorous.

59. The method of claim 47 wherein removing said spacer includes etching said spacer.

60. The method of claim 47 further comprising forming a capping layer on the substrate assembly.

61. A method of forming a semiconductor structure with a gate on a substrate assembly, comprising:

forming a sacrificial layer on the substrate assembly;

removing a portion of said sacrificial layer to form at least one spacer adjacent said gate;

forming raised source and drains on the substrate assembly;

removing said spacer; and

forming a capping layer on the substrate assembly.

62. The method of claim 61 wherein forming a capping layer includes forming an insulative layer.

63. The method of claim 61 wherein forming a capping layer includes forming an oxide layer.

64. The method of claim 61 wherein forming a capping layer includes depositing an oxide layer.

65. The method of claim 61 further comprising forming an insulative layer on the substrate assembly.

66. The method of claim 61 further comprising forming a doped oxide insulative layer on the substrate assembly.

67. A method of forming a semiconductor structure with a gate on a substrate assembly, comprising:

forming a sacrificial layer on the substrate assembly;

removing a portion of said sacrificial layer to form at least one spacer adjacent said gate;

forming raised source and drains on said substrate assembly;

removing said spacer to form a gap; and

forming a junction area beneath said gap and partially beneath said gate.

68. The method of claim 67 wherein forming a junction area includes implanting dopants beneath said gap and partially beneath said gate and one of said raised source and drains.

69. The method of claim 67 wherein forming a junction area includes implanting phosphorous beneath said gap and partially beneath said gate and one of said raised source and drains.

70. The method of claim 67 wherein forming a junction area includes forming a conductive layer on the substrate assembly.

71. The method of claim 67 wherein forming a junction area includes forming an outdiffusion area.

72. The method of claim 67 wherein forming a junction area includes implanting dopants.

73. The method of claim 67 wherein forming a junction area includes forming a shallow lightly doped area.

74. A method of forming a semiconductor structure having a gate on a substrate assembly, comprising:

forming a sacrificial layer on the substrate assembly;

removing a portion of said sacrificial layer to form at least one spacer adjacent said gate;

forming raised source and drains on said substrate assembly;

removing said spacer to form a gap;

forming a junction area substantially beneath said gap; and

forming a capping layer on the substrate assembly.

75. A method of forming a semiconductor structure with raised source and drains on a substrate assembly, the substrate assembly having a gate, comprising:

forming a gap between the source and the gate; and

forming a pocket implant beneath said gap and partially beneath the gate and the raised source.

76. The method of claim 75 wherein forming a pocket implant includes forming an outdiffusion area beneath the raised source.

77. A method of forming a semiconductor structure with raised source and drains on a substrate assembly, the substrate assembly having a gate, comprising:

forming a gap between the drain and the gate; and

forming a pocket implant substantially beneath said gap and partially beneath the gate and the raised drain.

78. The method of claim 77 wherein forming a pocket implant includes forming an outdiffusion area beneath the raised drain.

79. A method of creating a transistor on a substrate assembly, comprising:

forming a gate structure;

forming raised source and drain structures; and

forming junction areas in the substrate assembly between said gate structure and said raised source structure and between said gate structure and said raised drain structure, said junction areas extending beneath said gate structure and said raised source and drains.

80. The method of claim 79 wherein forming a gate structure includes forming a doped polysilicon layer on the substrate assembly.

81. The method of claim 80 wherein forming a layer of doped polysilicon includes chemically vapor depositing a polysilicon layer and doping said polysilicon layer with phosphorous.

82. A method of forming a transistor on a substrate assembly, comprising:

forming an oxide layer on a substrate layer;

forming a doped polysilicon layer on said oxide layer;

removing portions of said doped polysilicon layer to form a gate;

forming a sacrificial layer on the substrate assembly;

removing portions of said sacrificial layer to form a plurality of spacers adjacent said gate;

removing portions of said oxide layer;

forming a polysilicon layer on the substrate assembly;

planarizing said substrate assembly;

removing portions of said polysilicon layer to form a raised source and a raised drain;

forming a conductive layer on the substrate assembly;

doping said polysilicon layer;

removing portions of said conductive layer;

removing said spacers to create a plurality of gaps;

doping said substrate layer beneath said gaps;

forming a capping layer on said substrate assembly; and

forming an insulative layer on said substrate assembly.

83. The method of claim 82 wherein forming a conductive layer includes depositing a titanium layer.

84. The method of claim 82 wherein forming an insulative layer includes forming a PSG layer.

85. The method of claim 82 wherein forming an insulative layer includes forming a BPSG layer.

86. The method of claim 82 further comprising planarizing the substrate assembly after forming an insulative layer.

87. The method of claim 82 further comprising forming contact areas on the substrate assembly after forming said insulative layer.

88. The method of claim 87 further comprising forming an adhesion layer on the substrate assembly after forming contact areas.

89. The method of claim 82 further comprising forming at least one metallization layer on said substrate assembly after forming said insulative layer.

90. The method of claim 89 wherein forming at least one metallization layer includes forming at least one aluminum layer.

91. The method of claim 89 wherein forming at least one metallization layer includes forming at least one copper layer.

92. The method of claim 82 further comprising RTP sintering the substrate assembly after doping said substrate layer substantially beneath said gaps.

93. The method of claim 92 further comprising RTP annealing the substrate assembly after RTP sintering the substrate assembly.

94. A semiconductor device, comprising:

a substrate assembly;

at least one raised source;

at least one raised drain; and

at least one gate located between said source and said drain, said gate defining a first gap between said gate and said source, and said gate defining a second gap between said gate and said drain.

95. A semiconductor device, comprising:

a substrate assembly;

at least one raised source;

at least one raised drain;

at least one gate located between said source and said drain, said gate defining a first gap between said gate and said source, and said gate defining a second gap between said gate and said drain;

a first junction area located in said substrate assembly beneath said first gap; and

a second junction area located in said substrate assembly beneath said second gap.

96. A system, comprising:

a memory device having at least one semiconductor structure, said structure including:

a raised source;

a raised drain; and

a gate located between said source and said drain, said gate defining a first gap between said gate and said source, and said gate defining a second gap between said gate and said drain;

a processor; and

a bus connecting said processor and said memory device.

97. A system, comprising:

a memory device having at least one semiconductor structure formed on a substrate assembly, said structure including:

a raised source;

a raised drain;

a gate located between said source and said drain, said gate defining a first gap between said gate and said source, and said gate defining a second gap between said gate and said drain;

a first junction area located in the substrate assembly beneath said first gap; and

a second junction area located in the substrate assembly beneath said second gap;

a processor; and

a bus connecting said processor and said memory device.